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(71) Applicant(s)
Sharp Kabushiki Kaisha
(Incorporated in Japan)
22-22 Nagaike-cho, Abeno-ku, Osaka 545-8522, Japan

The Secretary Of State For Defence In Her Britannic Majesty's
(Incorporated in the United Kingdom)
Defence Evaluation And Research Agency, FARNBOROUGH, Hants, GU14 6TD, United Kingdom

(72) Inventor(s)
Takaji Numao

(74) Agent and/or Address for Service
Marks & Clerk
4220 Nash Court, Oxford Business Park South, OXFORD, OX4 2RU, United Kingdom

(54) Abstract Title
Display device using time division grey scale display method

(57) A plasma display pannel or liquid crystal display for providing a multi-greyscale display by forming a single field from n subfields the durations of which are in the ratio $1: \ldots :2^m: \ldots : (2^A-B)\times 2^k: \ldots$ where $1<m<A-1$, $0<k<n-A-1$, $A>1$, and $B>0$. There are two different ways of combining these subfields to produce a given greyscale. Which is selected is determined either by the grey levels of surrounding pixels or by whether the intensity of the pixel is increasing or decreasing. Alternatively, the ratio may be $1: (M^A-B)\times M^k: \ldots$ or $1: \ldots :M^m: \ldots : (M^A-B)\times M^k: \ldots$ where $M>2$ and $A>0$.

FIG.1(a)

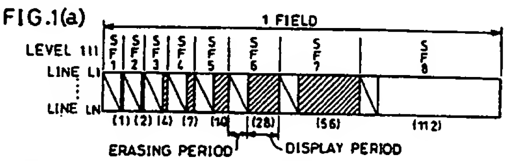


FIG. 1(b)

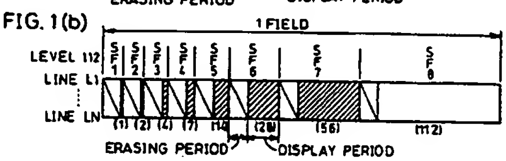


FIG.1(c)

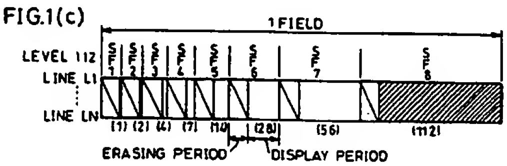
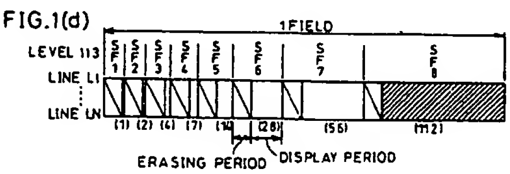


FIG.1(d)



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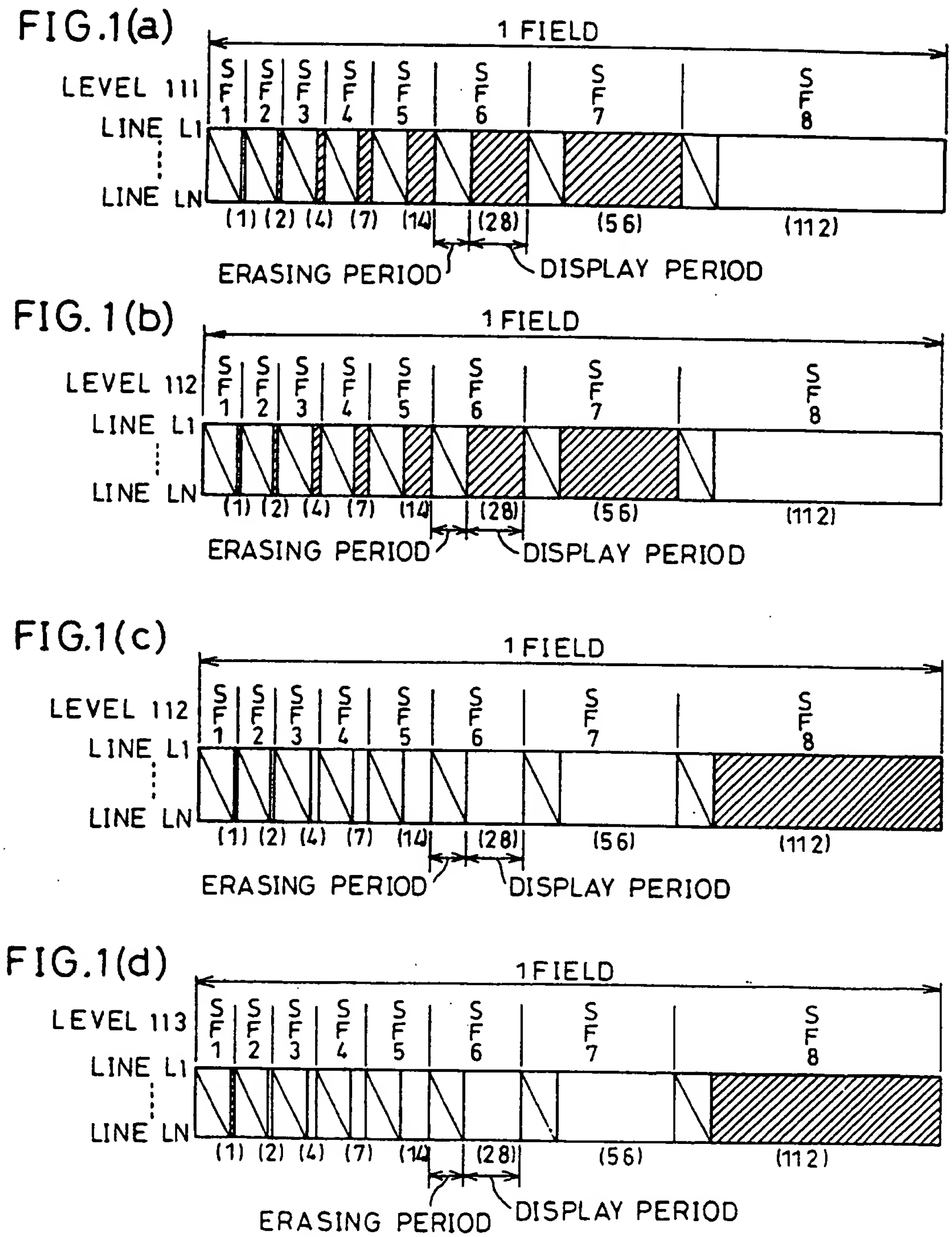


FIG.1(a)
1 FIELD
LEVEL 111
SF1 SF2 SF3 SF4 SF5 SF6 SF7 SF8
LINE L1
LINE LN
(1) (2) (4) (7) (14) (28) (56) (112)
ERASING PERIOD
DISPLAY PERIOD
FIG. 1(b)
1 FIELD
LEVEL 112
SF1 SF2 SF3 SF4 SF5 SF6 SF7 SF8
LINE L1
LINE LN
(1) (2) (4) (7) (14) (28) (56) (112)
ERASING PERIOD
DISPLAY PERIOD
FIG.1(c)
1 FIELD
LEVEL 112
SF1 SF2 SF3 SF4 SF5 SF6 SF7 SF8
LINE L1
LINE LN
(1) (2) (4) (7) (14) (28) (56) (112)
ERASING PERIOD
DISPLAY PERIOD
FIG.1(d)
1 FIELD
LEVEL 113
SF1 SF2 SF3 SF4 SF5 SF6 SF7 SF8
LINE L1
LINE LN
(1) (2) (4) (7) (14) (28) (56) (112)
ERASING PERIOD
DISPLAY PERIOD

FIG.2

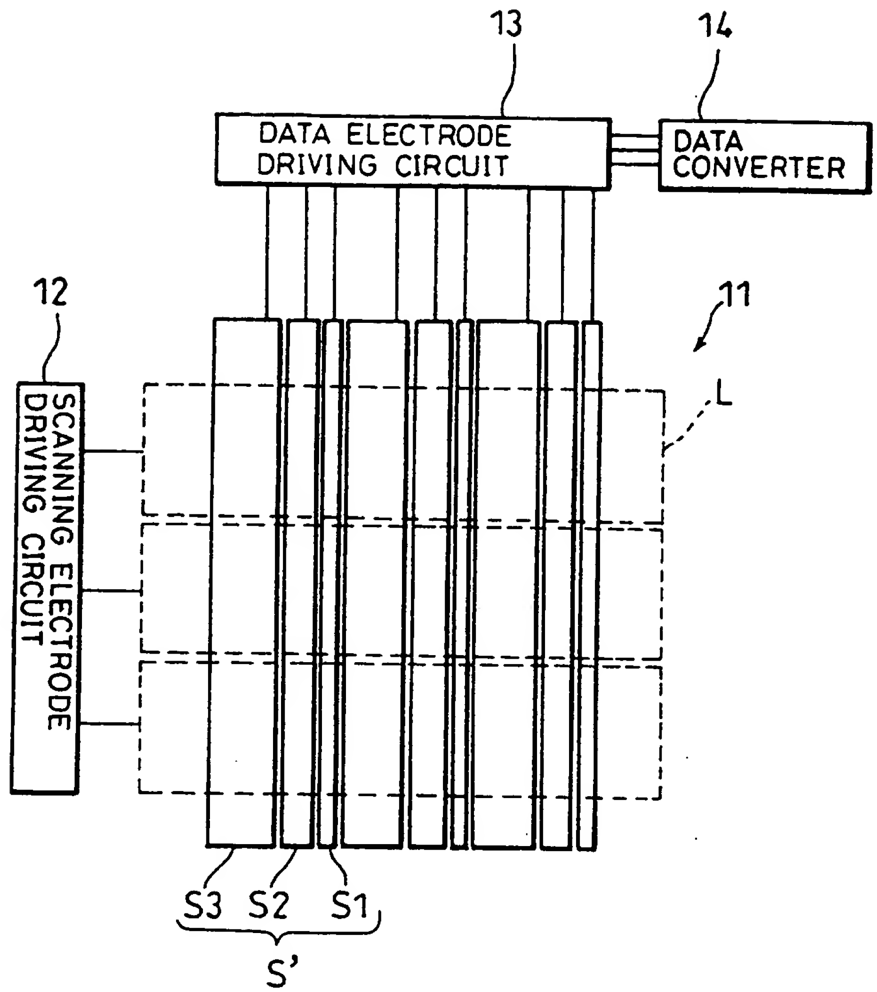
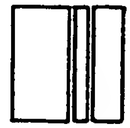
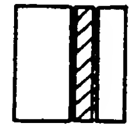

13
14
DATA ELECTRODE DRIVING CIRCUIT
DATA CONVERTER
12
11
SCANNING ELECTRODE DRIVING CIRCUIT
L
S3
S2
S1
S'

FIG.3(a)



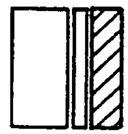
000

FIG.3(b)



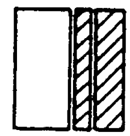
001

FIG.3(c)



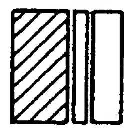
010

FIG.3(d)



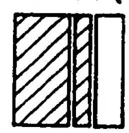
011

FIG.3(e)



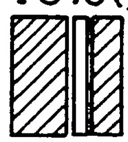
100

FIG.3(f)



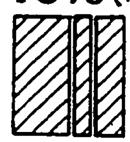
101

FIG.3(g)



110

FIG.3(h)



111

FIG.4

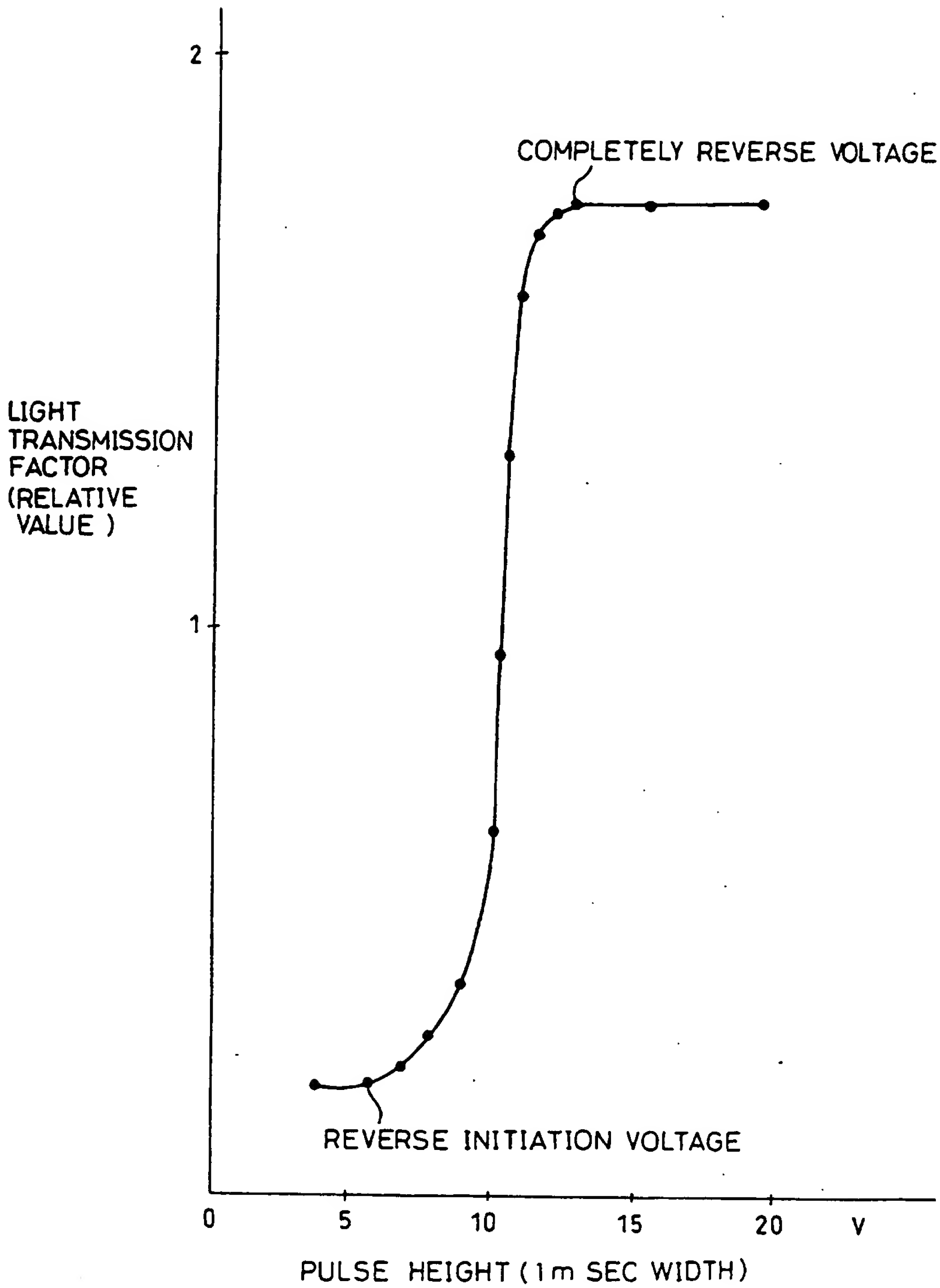
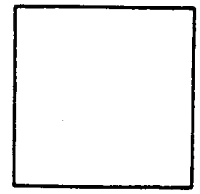
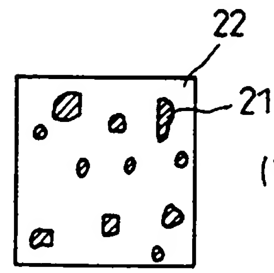

LIGHT TRANSMISSION FACTOR (RELATIVE VALUE)
2
1
COMPLETELY REVERSE VOLTAGE
REVERSE INITIATION VOLTAGE
0
5
10
15
20
V
PULSE HEIGHT (1 m SEC WIDTH)

FIG.5(a)



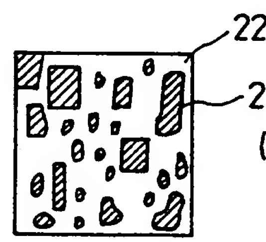
($V_0 - V_4 = 5V$)

FIG.5(b)



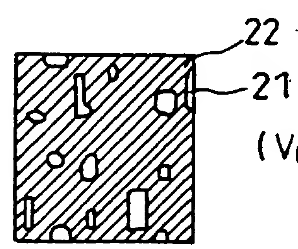
($V_0 - V_3 = 9V$)

FIG.5(c)



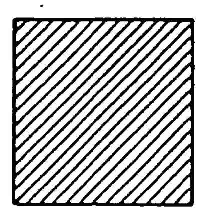
($V_0 - V_2 = 10.2V$)

FIG.5(d)



($V_0 - V_1 = 11V$)

FIG.5(e)



($V_0 = 15V$)

FIG.6(a)
LEVEL 55

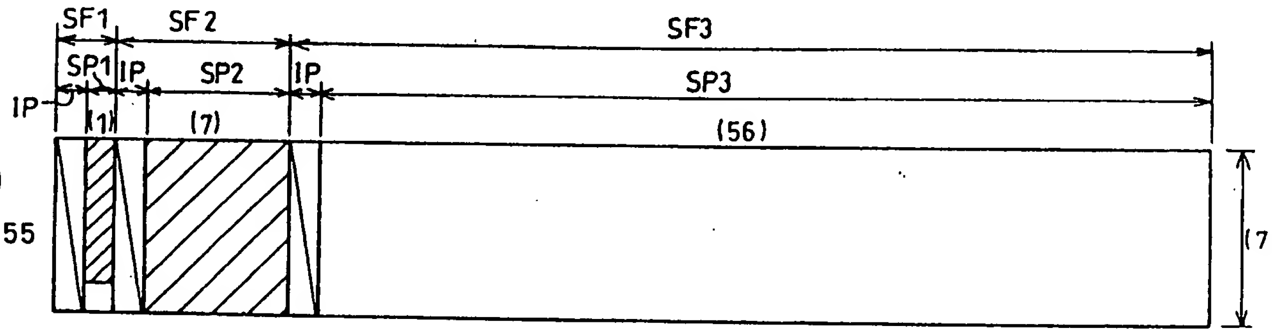


FIG.6(b)
LEVEL 56

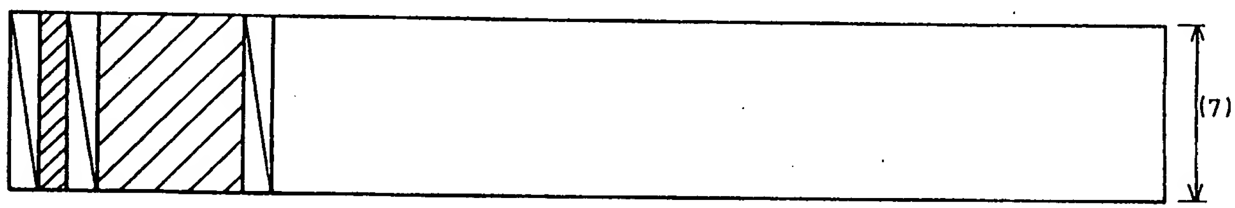


FIG.6(c)
LEVEL 56

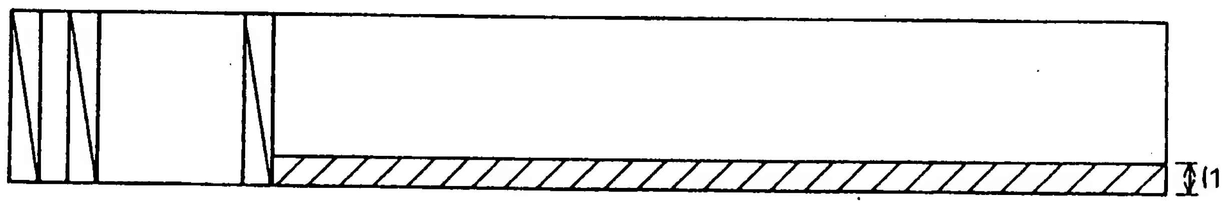


FIG.6(d)
LEVEL 57

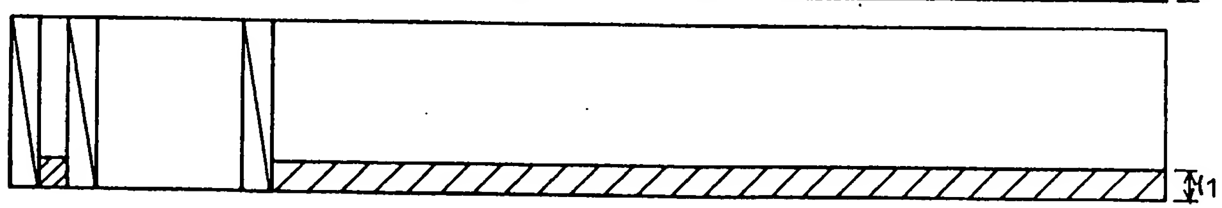


FIG.7

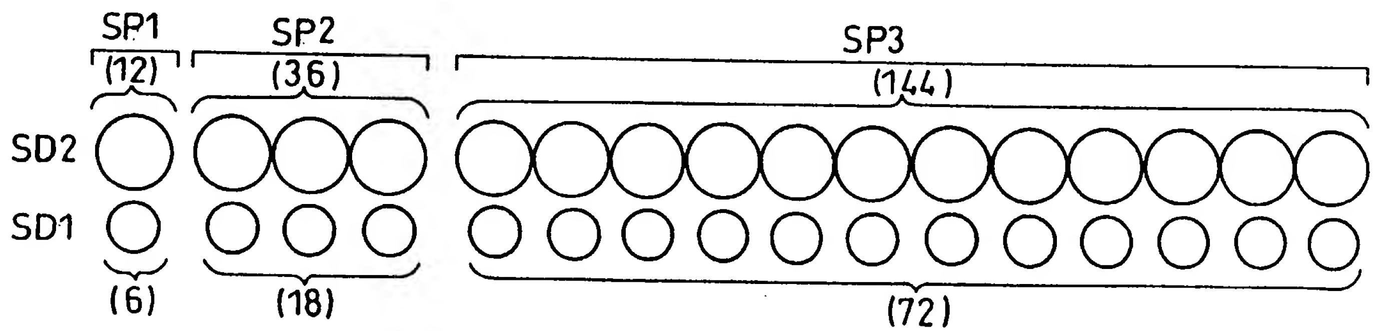
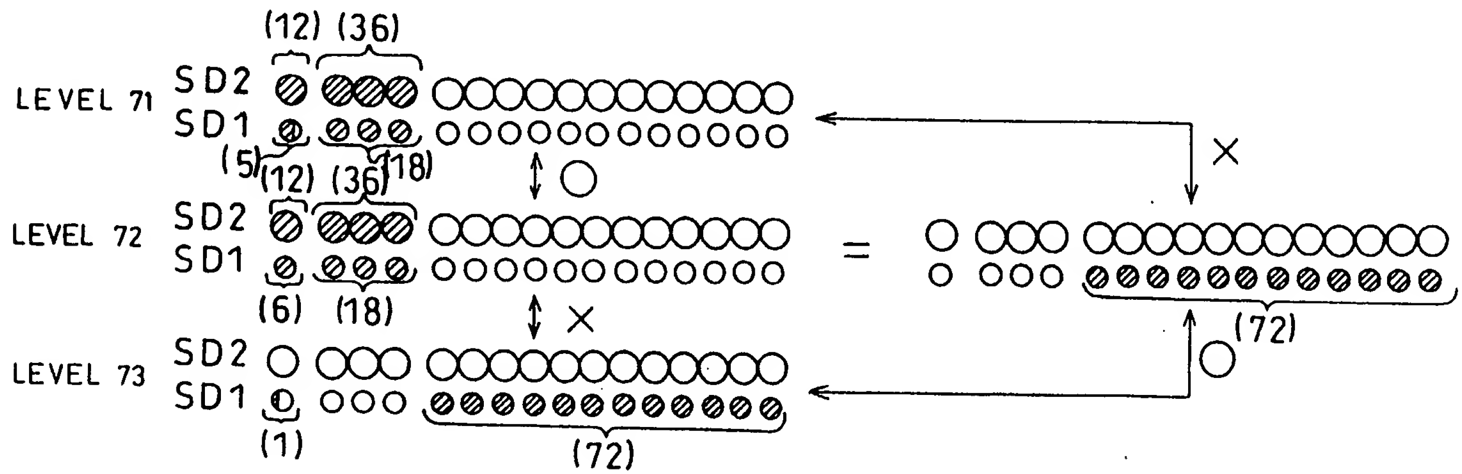


FIG.8



(12) (36)
LEVEL 71
SD2
SD1
(5)
(18)
(12) (36)
LEVEL 72
SD2
SD1
(6)
(18)
LEVEL 73
SD2
SD1
(1)
(72)
=
(72)

FIG.9

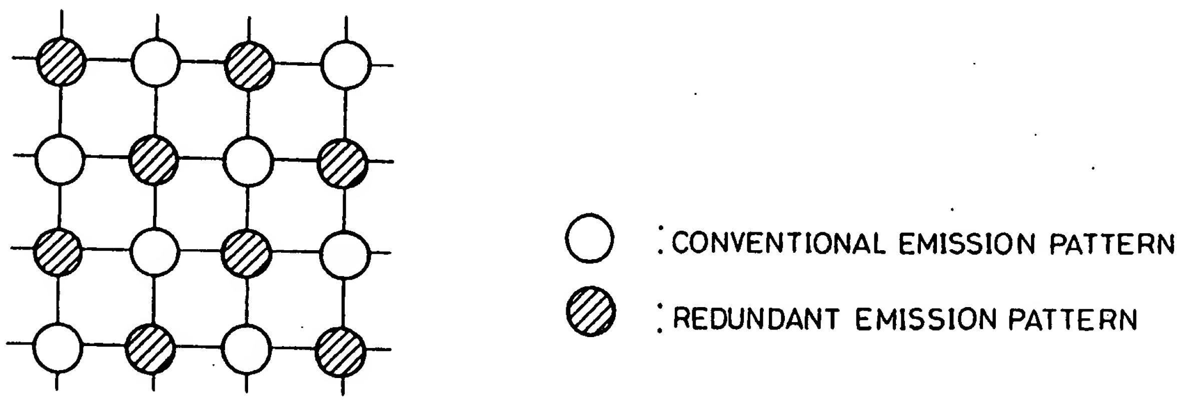

: CONVENTIONAL EMISSION PATTERN
: REDUNDANT EMISSION PATTERN

FIG.10

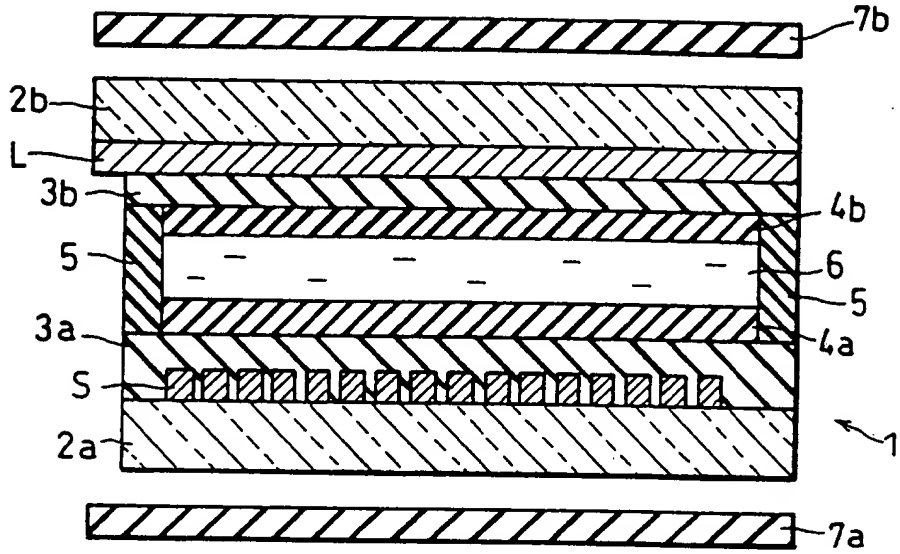


FIG. 11

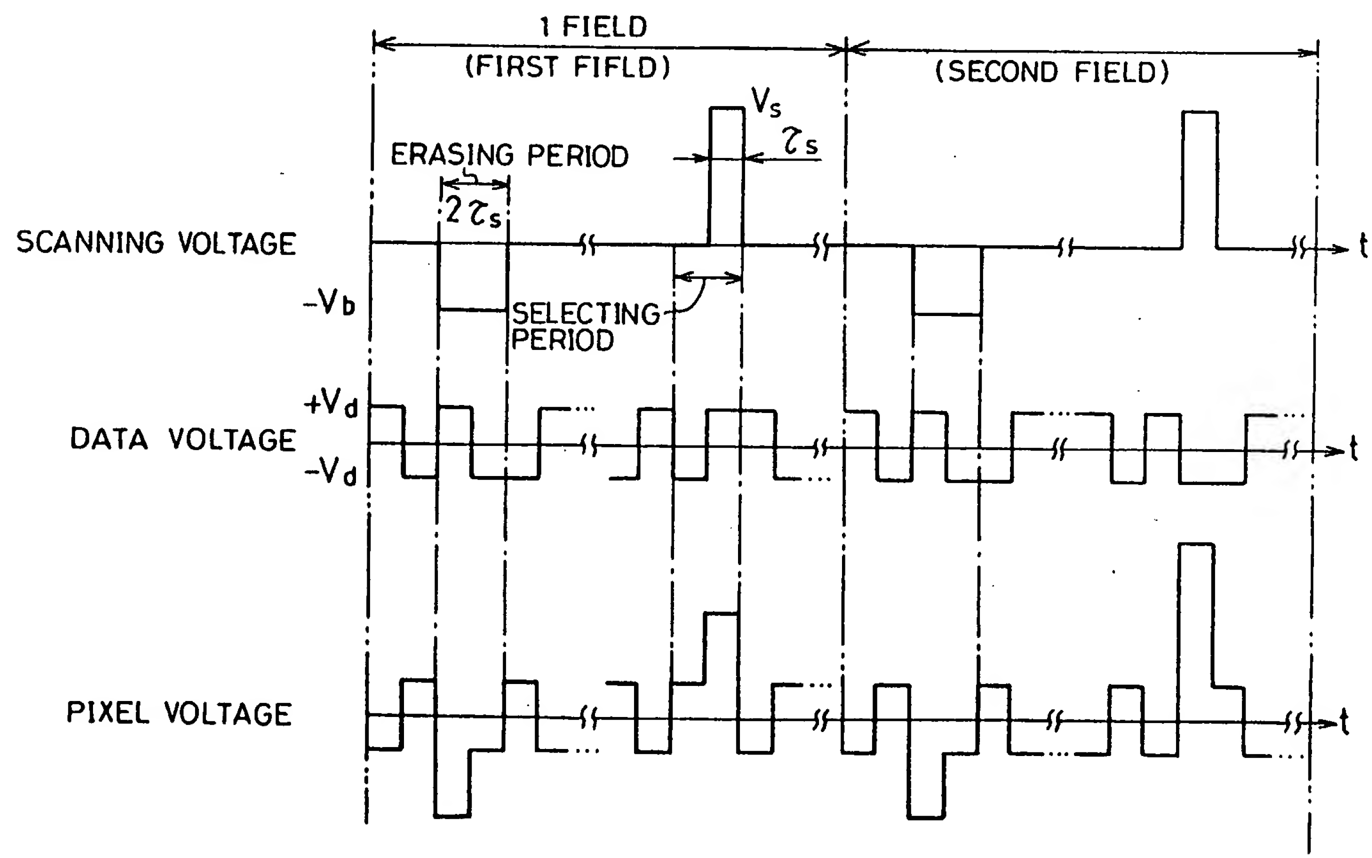

1 FIELD
(FIRST FIFLD)
(SECOND FIELD)
ERASING PERIOD
$2\tau_s$
V_s
τ_s
SCANNING VOLTAGE
$-V_b$
SELECTING PERIOD
$+V_d$
DATA VOLTAGE
$-V_d$
PIXEL VOLTAGE
t
t
t

FIG.12

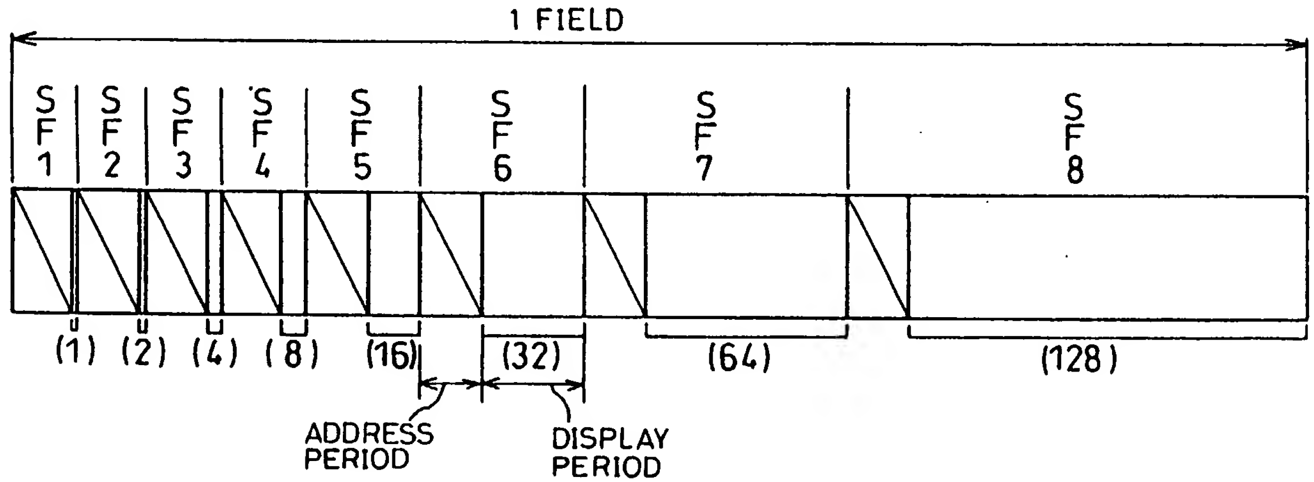

1 FIELD
SF1
SF2
SF3
SF4
SF5
SF6
SF7
SF8
(1)
(2)
(4)
(8)
(16)
(32)
(64)
(128)
ADDRESS PERIOD
DISPLAY PERIOD

FIG.13

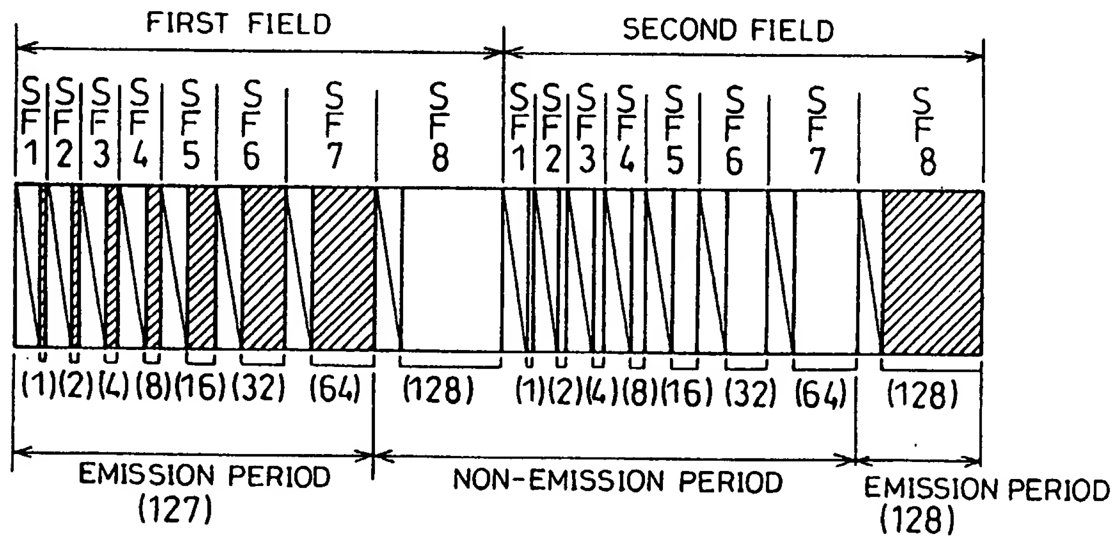

FIRST FIELD
SECOND FIELD
SF1 SF2 SF3 SF4 SF5 SF6 SF7 SF8
SF1 SF2 SF3 SF4 SF5 SF6 SF7 SF8
(1) (2) (4) (8) (16) (32) (64) (128)
(1) (2) (4) (8) (16) (32) (64) (128)
EMISSION PERIOD (127)
NON-EMISSION PERIOD
EMISSION PERIOD (128)

FIG.14

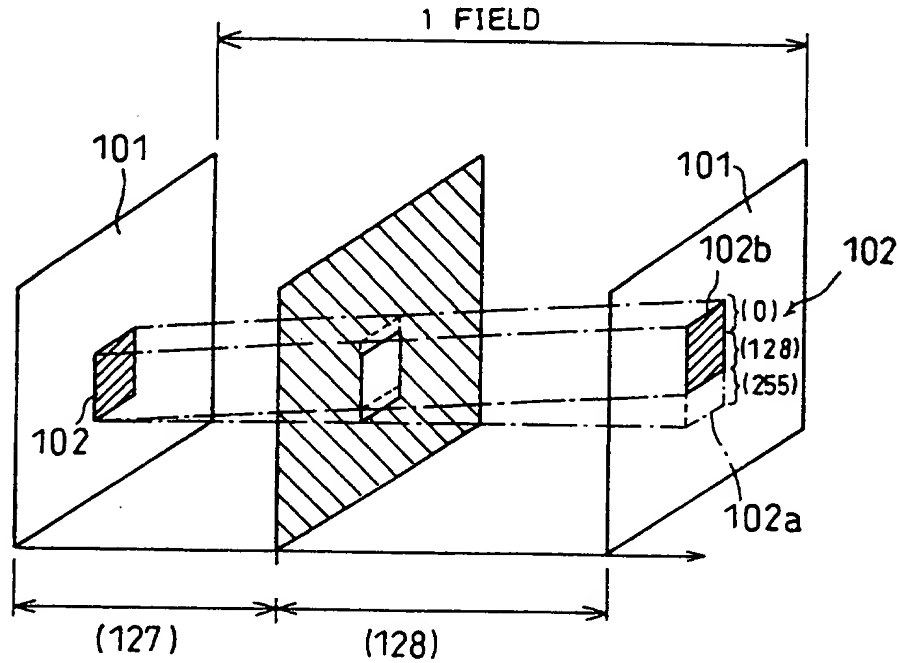


FIG.15

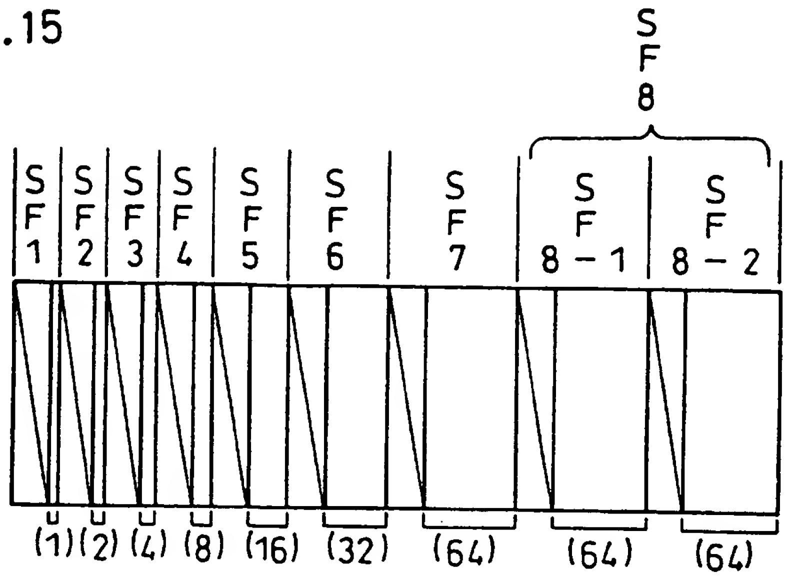

SF8
SF1
SF2
SF3
SF4
SF5
SF6
SF7
SF8-1
SF8-2
(1)
(2)
(4)
(8)
(16)
(32)
(64)
(64)
(64)

FIG.16


(48)
(48)
(1)
(2)
(4)
(8)
(16)
(32)
(48)
(48)

FIG.17(a)

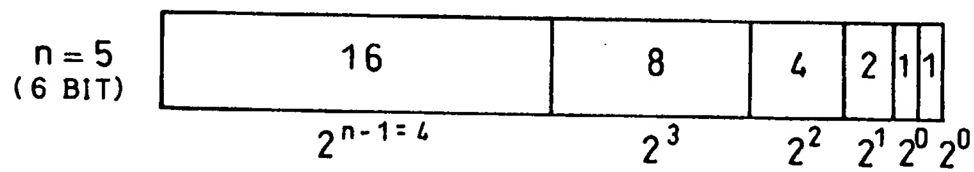


FIG.17(b)

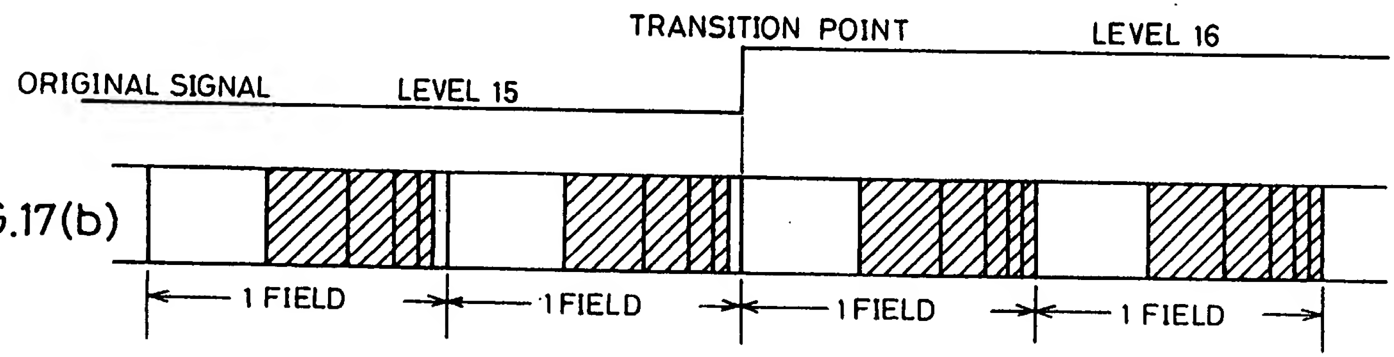
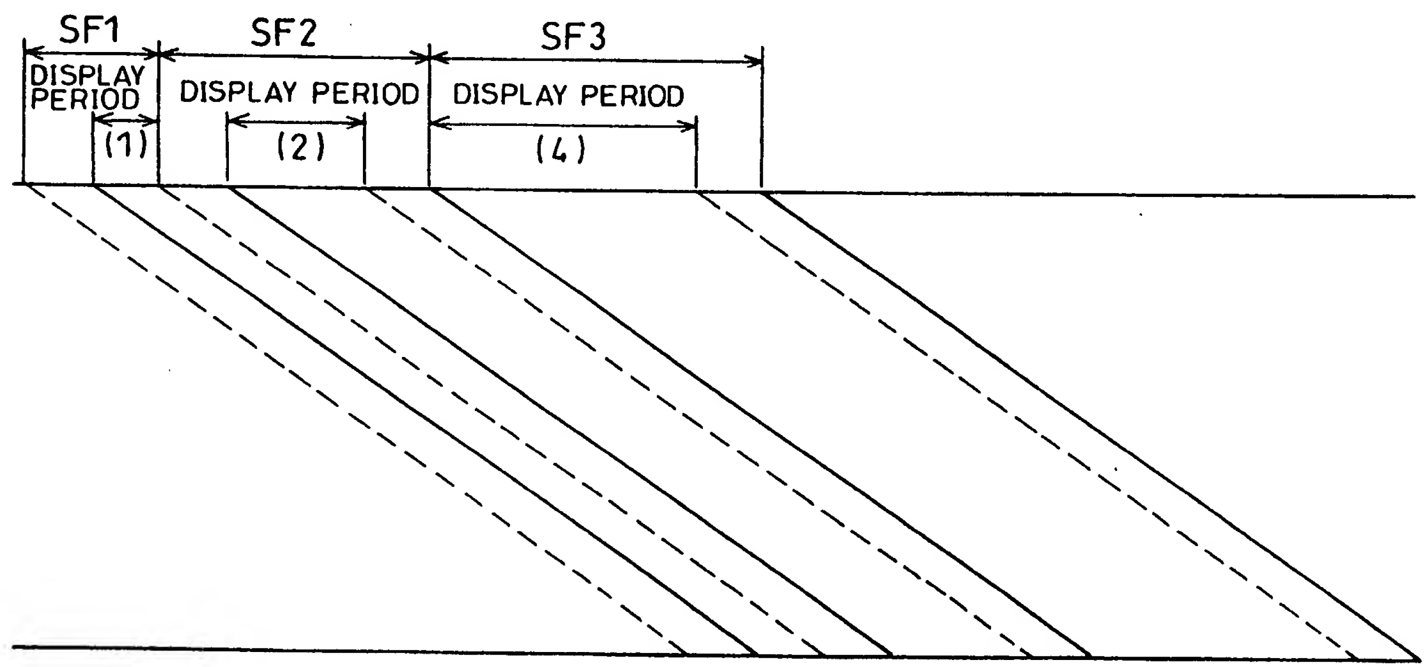


FIG.18


SF1
SF2
SF3
DISPLAY PERIOD
(1)
DISPLAY PERIOD
(2)
DISPLAY PERIOD
(4)

2327798

DISPLAY DEVICE

FIELD OF THE INVENTION

The present invention relates to display devices such as plasma display panels and ferroelectric liquid crystal display devices using a time division grey-scale display method.

BACKGROUND OF THE INVENTION

Display devices for producing substantially binary displays, such as a plasma display panel (hereinafter referred to as the "PDP") and a ferroelectric liquid crystal display device (hereinafter referred to as the "FLCD"), adopt a time division grey-scale display method in which scan of a plurality of sub-fields (or sub-frames) is performed

within one field period (or one frame period), and a grey-scale display is provided by the accumulative effect.

For example, in the PDP, as illustrated in Fig. 12, a single field period is divided into eight sub-field periods SF1 through SF8, and each sub-field period is further divided into an address period and a display period. The ratio of durations of the display periods of the sub-field periods SF1 through SF8 is arranged to be 1:2:4:8:16:32:64:128, and the display in each of the sub-field periods SF1 through SF8 is independently switched ON/OFF so as to realize a 256 grey-scale display.

However, in such a time division grey-scale display method, when displaying level 127, as shown in Fig. 13, the light emission periods corresponding to level 127 of the PDP concentrate in the front portion of a single field period. On the other hand, when displaying level 128, the emission periods concentrate in the rear portion of one-field period. In Fig. 13, the hatched portions indicate the light emission of the PDP.

Therefore, when a pixel changes from level 127 to level 128, a non-emission period in which the PDP does not emit light over a single field period is produced

at that moment. As a result, the pixel appears as a dark line in the displayed image, and thus degrades the image quality. On the other hand, the pixel appears as a bright line in the displayed image at a transition from the level 128 to level 127, resulting in degradation of the display quality.

In the case where the brightness of a still image alternately switches between the levels 127 and 128 (for example, in the case where the brightness to be exhibited is between level 127 and level 128, a single pixel takes the values of level 127 and level 128 level at random due to noise produced during analog-to-digital conversion in an A/D converter circuit), the moment at which the transition from level 127 to level 128 and the moment at which the transition from level 128 to level 127 are recognized as noise, resulting in considerable degradation of the image quality. Such a phenomenon will be referred to as the "spurious noise".

Moreover, as shown in Fig. 14, when an object 102 of a brightness of level 128 moves in a background 101 of a brightness of level 127, the viewer follows the moving object 102 of the brightness level 128 with eyes. Therefore, when the object 102 moves from an image 102a toward an image 102b, there is a

possibility that the object 102 whose brightness is actually level 128 is composed of a portion of brightness level 0, a portion of brightness level 128, and a portion of brightness level 255, and hence the image quality is considerably degraded. Such a phenomenon will be referred to as the "false contour".

In order to solve the above-mentioned problems, Japanese publication of unexamined patent application (Tokukaihei) No. 7-175439/1995 discloses a method in which one high-order bit that is the sub-field with a duration ratio of 128 of the conventional technique shown in Fig. 12 is further divided into two 64:64 sub-fields, namely, SF8-1 and SF8-2, as shown in Fig. 15. This method will be referred to as the "high-order-bit division technique".

Additionally, according to the disclosure of Mikoshiba, the University of Electronic Communication, "Dynamic False Contours on PDPs-Fatal or Curable?" IDW '96 Workshop on Plasma Displays, pp. 251-254, there is a method in which the two sub-fields of duration ratios of "64" and "128" shown in Fig. 12 are further divided into four 48:48:48:48 sub-fields as illustrated in Fig. 16, and then the sub-fields are relocated in the front portion and rear portion of a single field period. This method will be referred to

as the "sub-fields relocation technique". In this case, the bits are turned on by controlling the four sub-fields with durations of a ratio of "48" to emit light sequentially from the mean position of the one-field period so that a noticeable shift in the mean position of the emission periods is prevented.

Furthermore, Japanese publication of unexamined patent application (Tokukaihei) No. 8-278767/1996 discloses a grey-scale display method in which a sub-field with a duration ratio of "1" is added next to a sub-field with the duration ratio "1" corresponding to the lowest-order bit as shown in Fig. 17(a) (hereinafter referred to as the "lowest-order field addition technique"). In this case, the newly added lowest-order bit is turned on only when a transition from level 2^n-1 (for example, 15, if n=5) to level 2^n (for example, 16) at which the shift in the mean position of the emission periods of one pixel is large occurs, thereby reducing the shift in the mean position of the emission periods.

By the way, the above-mentioned spurious noise and false contour have been recognized as the problems unique to PDPs. However, it was found from the results of some experiments that such problems are common to both the PDPs and the display devices for

performing time division grey-scale displays.

For example, similarly to the PDP, in a FLCD, as shown in Fig. 18, a single field period is divided into three sub-field periods, namely, SF1 through SF3, and each sub-field period is further divided into an erasing period and a display period. The ratio of durations of the display periods of the sub-field periods SF1 through SF3 is arranged to be 1:2:4, and the display in each of the sub-field periods SF1 through SF3 is independently switched between ON and OFF so as to realize an 8-grey-scale display. However, it was found recently that spurious noise and false contour occur in the FLCD like in the PDP, if the FLCD employs the time division grey-scale display method.

Therefore, it was considered to use the conventionally proposed high-order-bit division technique, sub-fields relocation technique, or lowest-order field addition technique, which can reduce spurious noise and false contour. However, with the use of any of these techniques, the number of necessary sub-fields increases.

This is a critical drawback for a display device, for example, the FLCD, in which capacitive load (i.e., ferroelectric liquid crystal) is driven.

Specifically, in the FLCD, a scanning voltage shown in the first row of Fig. 11 that explains the present invention is applied to a scanning electrode L of the FLCD (see Fig. 10 showing the present invention), a data voltage shown in the second row of Fig. 11 is applied to a data electrode S (see Fig. 10), and a pixel voltage shown in the third row of Fig. 11 is applied to a ferroelectric liquid crystal (hereinafter referred to as the "FLC") 6 (see Fig. 10) placed between the scanning electrode L and data electrode S so as to drive the FLC. The pixel voltage is the differential voltage of the scanning voltage and data voltage. Therefore, as the driving frequency becomes higher, the occurrence of problems such as waveform distortion at the end of the electrodes and generation of heat due to a current flowing in the electrodes increases.

Moreover, in the FLCD, the scanning period is given by the equation,

1 scanning period = 1 field period/(number of scanning lines × number of sub-fields).

In display devices such as HDTV and XGA having a large number of scanning lines, one scanning period becomes too short, and therefore an appropriate number of sub-fields cannot be ensured.

For example, if the number of sub-fields is arranged to be eight in all of the techniques due to such a restriction on the scanning period, a 256-grey-scale display is achieved by the time division grey-scale display with a ratio of durations of the display periods of 1:2:4:8:16:32:64:128 according to the conventional technique. On the contrary, in the high-order-bit division technique, only a 128-grey-scale display is provided by the time division grey-scale display with a ratio of durations of the display periods of 1:2:4:8:16:32:32:32. Similarly, according to the sub-fields relocation technique, only a 64-grey-scale display is provided by the time division grey-scale display with a ratio of durations of the display periods of 16:16:1:2:4:8:16:16. Furthermore, according to the lowest-order field addition technique, only a 129-grey-scale display is provided by the time division grey-scale display with a ratio of durations of the display periods of 1:1:2:4:8:16:32:64.

SUMMARY OF THE INVENTION

In order to solve the above problems, it is an object of the present invention to provide a display device capable of displaying an increased number of

grey levels compared with the above-mentioned three techniques when using the same number of sub-fields as in the conventional technique shown in Fig. 12, and of reducing the problems such as spurious noise and false contour associated with the time-division grey-scale display.

In order to achieve the object, a first display device of the present invention is a display device for producing a multi-grey-scale display by forming a single field from a plurality of sub-fields which are different from each other in durations of display periods thereof, and arranging the ratio of the durations of the display periods corresponding to the respective sub-fields so that

$$1 : \ldots : 2^m : \ldots : (2^A - B) \times 2^k : \ldots$$

where m represents a variable between 1 and A-1, k represents a variable between 0 and n-A-1, n represents the number of the sub-fields, A represents an integer of not less than 2, and B represents an integer of not less than 1.

When the structure of the first display device is adopted into a device in which each pixel can display two levels without time dither technique, the time-division grey-scale display can be obtained by independently switching each sub-field period between

ON and OFF. At this time, if ON/OFF of each sub-field period is appropriately controlled according to a change in the brightness of the image in a time-axis direction, when the same number of sub-fields as in the conventional structures is used, the structure of the first display device can exhibit an significantly increased number of grey levels as compared with the conventional structures, without causing problems such as spurious noise and false contour associated with the time division grey-scale display. In particular, it is possible to effectively reduce the occurrence of spurious noise and false contour during a transition from level $(2^A-B)\times2^k-B$ to level $(2^A-B)\times2^k$ or from level $(2^A-B)\times2^k+B$ to level $(2^A-B)\times2^k$ in which a large shift in the mean position of the display periods showing a bright image occurs.

In order to achieve the above object, a second display device of the present invention is a display device for producing a multi-grey-scale display by forming a single field from a plurality of sub-fields which are different from each other in durations of display periods thereof and arranging the ratio of the durations of the display periods corresponding to the respective sub-fields so that

$1 : (M^A-B)\times M^k : \ldots,$

or

$$1 : \ldots : M^m : \ldots : (M^A - B) \times M^k : \ldots$$

where M (M being an integer of not less than 3) represents the number of grey levels displayable in each of the sub-field periods corresponding to bits other than the lowest-order bit, m represents a variable between 1 and A-1, k represents a variable between 0 and n-A-1, n represents the number of the sub-fields, A represents an integer of not less than 1, and B represents an integer of not less than 1.

When this structure is adopted into a display device in which a single pixel can display M grey levels without time dither technique, the same effect as that of the structure of the first display device is obtained.

For a fuller understanding of the nature and advantages of the invention, reference should be made to the ensuing detailed description taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1(a), 1(b), 1(c) and 1(d) are views for explaining time-division grey-scale display of a display device according to Embodiment 1 of the present invention, wherein Fig. 1(a), 1(b), 1(c), 1(d)

show level 111, level 112 of the redundant emission pattern, level 112 of the conventional emission pattern, and level 113, respectively.

Fig. 2 is a view showing the structure of a display device according to Embodiment 2 of the present invention.

Figs. 3(a), 3(b), 3(c), 3(d), 3(e), 3(f), 3(g) and 3(h) are views for explaining grey-scale display performed by dividing a single data electrode of the display device into a plurality of sub-data-electrodes.

Fig. 4 is a graph showing the relationship between a pulse voltage to be applied to the data electrode of the display device and a light transmission factor.

Figs. 5(a), 5(b), 5(c), 5(d) and 5(e) are views for explaining grey-scale display performed by varying the pulse voltage in the display device.

Figs. 6(a), 6(b), 6(c) and 6(d) are views for explaining a combination of pixel division grey-scale display and time division grey-scale display.

Fig. 7 is a view for explaining a combination of pixel division grey-scale display, grey-scale display performed by varying the pulse voltage, and time division grey-scale display.

Fig. 8 is a view for explaining three levels of the time division grey-scale display of Fig. 7.

Fig. 9 is a view for explaining the spatial distribution of the time division grey-scale display.

Fig. 10 is a view showing the structure of a ferroelectric liquid crystal display device of Embodiment 1.

Fig. 11 is a waveform chart for showing a driving scheme of the ferroelectric liquid crystal display device.

Fig. 12 is a view for explaining a time division 256-grey-scale display of a plasma display panel using a conventional technique.

Fig. 13 is a view for explaining a problem in a still image of the time division 256-grey-scale display.

Fig. 14 is a view for explaining a problem in a moving image of the time division 256-grey-scale display.

Fig. 15 is a view for explaining a time division 256-grey-scale display of a plasma display panel using a high-order-bit division technique.

Fig. 16 is a view for explaining a time division 256-grey-scale display of a plasma display panel using a sub-fields relocation technique.

Figs. 17(a) and 17(b) are views for explaining a time division 256-grey-scale display of a plasma display panel using a lowest-order bit addition technique.

Fig. 18 is a view for explaining a time division 256-grey-scale display of a ferroelectric liquid crystal display device using the conventional technique.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[Embodiment 1]

The following description will explain an embodiment of the present invention with reference to Figs. 1, 10 and 11. In this embodiment, the present invention is applied to a ferroelectric liquid crystal display device (hereinafter referred to as the "FLCD").

[Basic Structure of FLCD]

As illustrated in Fig. 10, the FLCD according to this embodiment has a liquid crystal panel 1. The liquid crystal panel 1 includes two facing light-transmitting substrates made of, for example, glasses.

A plurality of transparent data electrodes S made of, for example, indium tin oxide (hereinafter

referred to as "ITO") are arranged parallel to each other on a surface of the substrate 2a. These data electrodes S are covered with a transparent insulating film 3a made of, for example, silicon dioxide (SiO_2).

On the other hand, a plurality of transparent scanning electrodes L made of, for example, ITO are arranged parallel to each other on a surface of the substrate 2b so as to cross the data electrodes S at right angles. These scanning electrodes L are covered with a transparent insulating film 3b made of the same material as the insulating film 3a.

The scanning electrodes L and data electrodes S arranged to cross each other at right angles form a plurality of pixels arranged in a matrix pattern.

Alignment films 4a and 4b which have undergone a uniaxial alignment process such as rubbing process are placed on the insulating films 3a and 3b, respectively. As the alignment films 4a and 4b, polyvinyl alcohol, etc. is used.

The substrates 2a and 2b are fastened together with a sealing material 5 so that the alignment films 4a and 4b face each other. The ferroelectric liquid crystal 6 is injected from an inlet provided in the sealing material 5, and sealed in the space between the substrates 2a and 2b by closing the inlet. The

ferroelectric liquid crystal 6 fills up the space and forms a liquid crystal layer.

The substrates 2a and 2b are sandwiched between two polarizing plates 7a and 7b which are disposed so that their polarization axes cross each other at right angles.

[Driving Scheme of FLCD]

Referring now to Fig. 11, the following description will explain driving the FLCD by a blanking driving scheme.

The top row in Fig. 11 shows the waveform of a scanning voltage applied to the scanning electrode L by the blanking driving scheme. As clear from this waveform, according to the blanking driving scheme, a single field period includes a selecting period of two slots ($2\tau_s$), and a 2-slot erasing period of a length equal to that of the selecting period before the selecting period.

The peak value of the first slot of the selecting period is 0 V, and a strobe pulse of a peak value V_s is applied as the scanning voltage in the second slot. In the erasing period, a strobe pulse which has a polarity opposite to the above-mentioned strobe pulse, a 2-slot pulse width and a peak value V_b is applied.

For example, as shown in the middle row of Fig. 11, a data voltage to be applied to the data electrode S is expressed by a bipolar pulse with a cycle of two slots. The data voltage is arranged so that the first slot is $-V_d$ and the second slot is $+V_d$ in writing, and that the first slot is $+V_d$ and the second slot is $-V_d$ in non-writing.

The potential difference between the scanning voltage and data voltage is applied to the pixel. The lowest row in Fig. 11 shows the waveform of a pixel voltage produced in the pixel by the scanning voltage and data voltage.

[Time Division Grey-Scale Display Method of FLCD]

The time division grey-scale display method explained in this embodiment is an example when the weighing factor of the time division grey-scale display (when the number (M) of grey levels displayable in the sub-field period equivalent to each of bits other than the lowest-order bit) is two, i.e., when one pixel provides a binary display.

Here, a single field period is divided into n sub-field periods SF1 through SFn, and each sub-field period is composed of an erasing period and a display period.

The ratio of durations of the display periods corresponding to the sub-field periods SF1 through SFn is given by formula (1),

$$1 : \ldots : 2^m : \ldots : (2^A-B)\times 2^k : \ldots \qquad \ldots (1),$$

where m is a variable between 1 and A-1, k is a variable between 0 and n-A-1, n is the number of sub-fields, A is an integer not smaller than 2, and B is an integer not smaller than 1.

Fig. 1 explains the time division grey-scale display when n=8, A=3, and B=1. According to formula (1), the ratio of durations of the display periods SP1 through SP8 of the sub-field periods SF1 through SF8 is

$$1:2:2^2:(2^3-1):(2^3-1)\times 2:(2^3-1)\times 2^2:(2^3-1)\times 2^3:(2^3-1)\times 2^4$$
$$= 1:2:4:7:14:28:56:112.$$

At this time, the number of grey levels that can be displayed is 225.

In this case, it is considered that a large shift in the mean position of the bright display periods occurs, for example, on the following occasions:

① at a transition of display level from level $2+2^2=6$ to level $(2^3-1)=7$, or from level $1+2+2^2=7$ to level $1+(2^3-1)=8$;

② at a transition of the display level from level $2+2^2+(2^3-1)=13$ to level $(2^3-1)\times 2=14$, or from

level $1+2+2^2+(2^3-1)=14$ to level $1+(2^3-1)\times2=15$;

③ at a transition of the display level from level $2+2^2+(2^3-1)+(2^3-1)\times2=27$ to level $(2^3-1)\times2^2=28$, or from level $1+2+2^2+(2^3-1)+(2^3-1)\times2=28$ to level $1+(2^3-1)\times2^2=29$;

④ at a transition of the display level from level $2+2^2+(2^3-1)+(2^3-1)\times2+(2^3-1)\times2^2=55$ to level $(2^3-1)\times2^3=56$, or from level $1+2+2^2+(2^3-1)+(2^3-1)\times2+(2^3-1)\times2^2=56$ to level $1+(2^3-1)\times2^3=57$; and

⑤ at a transition of the display level from level $2+2^2+(2^3-1)+(2^3-1)\times2+(2^3-1)\times2^2+(2^3-1)\times2^3=111$ to level $(2^3-1)\times2^4=112$, or from level $1+2+2^2+(2^3-1)+(2^3-1)\times2+(2^3-1)\times2^2+(2^3-1)\times2^3=112$ to level $1+(2^3-1)\times2^4=113$.

Among these cases, the largest shift in the mean position of the bright display periods occurs at ⑤, namely the transition of display level from level 111 to level 112, or from level 112 to level 113.

According to an example shown in Figs. 1(a) to (d), at level 111, a bright display state is produced in the display periods of sub-field periods SF2 through SF7 (see Fig. 1(a)). At level 113, the bright display state is given in the display periods of sub-fields SF1 and SF8 (see Fig. 1(d)).

As the display state of level 112, both of the display state shown in Fig. 1(b) (hereinafter referred

to as the "redundant emission pattern") and the display state of Fig. 1(c) (hereinafter referred to as the "conventional emission pattern") exist. In the redundant emission pattern, the display period of each of the sub-field periods SF1 through SF7 is bright. Whereas, in the conventional emission pattern, the display period of the sub-field period SF8 is bright. The wording "conventional emission pattern" here used means "one pattern of a plurality of emission patterns for displaying the same level".

It should be understood from these display states that the largest shift in the mean position of the bright display periods occurs at a transition from level 111 to level 112 of the conventional emission pattern and a transition from level 112 to level 113 of the redundant emission pattern.

Therefore, when displaying the same level 112, it is judged whether the previous display state is a level not higher than level 111 or a level not lower than level 113. If the previous display state is a level not higher than level 111, the redundant emission pattern shown in Fig. 1(b) is used. On the other hand, if the previous display state is a level not lower than level 113, the conventional emission pattern shown in Fig. 1(c) is used. With this

structure, it is possible to limit the shift in the mean position of the display periods.

In formula (1), "A" determines the number of grey levels, and when the values of "M" (that is 2 in this case) and "B" are fixed, the number of grey levels becomes greater as the value of "A" increases.

For instance, when A=2 and B=1, the ratio of durations of the display periods is

$$1:2:(2^2-1):(2^2-1)\times2:(2^2-1)\times2^2:(2^2-1)\times2^3:(2^2-1)\times2^4:(2^2-1)\times2^5$$

$$= 1:2:3:6:12:24:48:96,$$

then a 193-grey-scale display is provided.

When A=4 and B=1, the ratio of durations of the display periods is

$$1:2:2^2:2^3:(2^4-1):(2^4-1)\times2:(2^4-1)\times2^2:(2^4-1)\times2^3$$

$$= 1:2:4:8:15:30:60:120,$$

then a 241-grey-scale display is provided.

Moreover, in formula (1), "B" determines the interval between levels having double patterns, i.e., the conventional emission pattern and redundant emission pattern (hereinafter referred to as the "double-patten interval"). When the values of "M" and "A" are fixed, the double-pattern interval becomes smaller as the value of "B" increases. For instance, as described above, when B=1, only one level every

$1+2+2^2=(2^3-1)=7$ levels has the conventional emission pattern and redundant emission pattern. On the other hand, when B=2, one level every $2+2^2=(2^3-2)=6$ levels has the conventional emission pattern and redundant emission pattern. Thus, as the value of "B" increases, the problems such as spurious noise and false contour associated with the time division grey-scale display decrease.

For example, when A=3 and B=2, the ratio of durations of the display periods is

$$1:2:2^2:(2^3-2):(2^3-2)\times 2:(2^3-2)\times 2^2:(2^3-2)\times 2^3:(2^3-2)\times 2^4$$
$$= 1:2:4:6:12:24:48:96,$$

then the double-pattern interval is six.

When A=3 and B=3, the ratio of durations of the display periods is

$$1:2:2^2:(2^3-3):(2^3-3)\times 2:(2^3-3)\times 2^2:(2^3-3)\times 2^3:(2^3-3)\times 2^4$$
$$= 1:2:4:5:10:20:40:80,$$

then the double-pattern interval is five.

As described above, in the display device of this embodiment for producing a multi-grey-scale display by forming one field from a plurality of sub-fields which are different from each other in durations of display periods, the ratio of durations of the display periods of the respective sub-field periods is arranged to satisfy above-mentioned formula (1).

With this arrangement, for example, when n=8, A=3, and B=1, the number of displayable grey levels is 225, thereby reducing the problems such as spurious noise and false contour associated with the time division grey-scale display. Assuming that the same number of sub-fields is used by each technique, the number of grey levels is 128 with the conventional high-order-bit division technique, 64 with the sub-fields relocation technique, and 129 with the lowest-order field addition technique. It can thus be understood that the number of displayable grey levels by the structure of the present invention is significantly increased as compared with these conventional techniques.

Moreover, when the display periods corresponding to n sub-field periods are denoted by SP1, SP2, ..., SPi, ..., SPn (i being an integer which is not smaller than A+1 but not greater than n), the display device of this embodiment has a first display state (for example, level 111) in which the display periods SP2 through SPi are bright, and the display periods SP1, SP(i+1) through SPn are dark; a second display state (for example, level 112 of the redundant emission pattern) in which the display periods SP1 through SPi are bright and the display periods SP(i+1) through SPn

are dark, the second display state having a brightness level next to the brightness level of the first display state; a third display state (for example, level 112 of the conventional emission pattern) in which the display period SP(i+1) is bright and the display periods SP1 through SPi, SP(i+2) through SPn are dark, the third display state having the same brightness level as the second display state; and a fourth display state (for example, level 113) in which the display periods SP1 and SP(i+1) are bright and the display periods SP2 through SPi, SP(i+2) through SPn are dark, the fourth display state having a brightness level next to the brightness level of the third display state.

Furthermore, when selecting the brightness level of the second or third display state, if the display state in the previous field of each pixel is not higher than the brightness level of the first display state, the second display state is selected as the next display state, and if it is not lower than the brightness level of the fourth display state, the third display state is selected as the next display state.

Therefore, a dark image or a bright line is not displayed over one field, thereby preventing

degradation of the image quality.

Regarding the order of sub-fields on time axis, in this embodiment, a sub-field corresponding to the shortest bit comes first. However, the present invention is not necessarily limited to such an order. In other words, the order of sub-fields on time axis can be arranged so that a sub-field corresponding to the longest bit comes first or sub-fields can be located in any order.

[Embodiment 2]

The following description will explain Embodiment 2 of the present invention with reference to Figs. 2 through 8. The same members as those shown in the figures of the above-mentioned embodiment will be designated by the same code and their description will be omitted.

This embodiment explains a display device such as FLCD which produces a binary display in substance, wherein the weighing factor of the time division grey-scale display (the number (M) of grey levels displayable in each of the sub-field periods equivalent to bits other than the lowest-order bit) is not smaller than three.

Here, a single field period is divided into n

sub-field periods SF1 through SFn, and each sub-field period is composed of an erasing period and a display period.

The ratio of durations of the display periods corresponding to the sub-field periods SF1 through SFn is given by formula

$$1 : (M^A-B) \times M^k : \ldots \qquad \ldots (2),$$

or

$$1 : \ldots : M^m : \ldots : (M^A-B) \times M^k : \ldots \qquad \ldots (3),$$

where m is a variable between 1 and A-1, k is a variable between 0 and n-A-1, n is the number of sub-fields, A is an integer not smaller than 1, and B is an integer not smaller than 1.

As a technique for determining "M", there are two methods. In the first method (pixel division grey-scale display method), a single pixel is divided into a plurality of sub-pixels. In the second method, the brightness of the pixel is changed by controlling a pulse voltage to be applied to the data electrode.

Referring now to Fig. 2 illustrating an FLCD, the following description will explain the first method.

This FLCD includes a liquid crystal panel 11 which has the same structure as the liquid crystal panel 1 of Embodiment 1, except the data electrodes S. More specifically, the liquid crystal panel 11

includes a plurality of scanning electrodes L, and a plurality of data electrodes S′ arranged to cross the scanning electrodes L at right angles. Moreover, the liquid crystal panel 11 is connected to a scanning electrode driving circuit 12 for applying a scanning voltage to the scanning electrodes L, and a data electrode driving circuit 13 for applying a data voltage to the data electrodes S. The data electrode driving circuit 13 is connected to a converter 14 for converting an input display grey level into a light emission pattern of the present invention.

Here, the data electrode S′ is divided into three sub-data-electrodes S1, S2 and S3 so that the ratio of the electrode widths is 1:2:4. By dividing a single pixel into three sub-pixels, as shown in Figs. 3(a) through 3(h), 8 grey levels (0 through 7) can be displayed in each sub-field period. In Figs. 3(a) through 3(h), the portions shown by hatching indicate a bright display state.

Whereas in the second method, for example, as shown in Fig. 4, a pulse voltage to be applied to the data electrodes of the FLCD is changed. In Fig. 4, the vertical axis indicates a relative value when the light transmission factor of one pulse height is 1.

With this structure, for example, as shown in

Figs. 5(a) through 5(e), since the ratio of a bright domain area 22 to a dark domain area 21 in a single pixel can be changed, it is possible to produce a display of three or more grey levels in each sub-field period.

Figs. 6(a) through 6(d) explain the time division grey-scale display produced by the FLCD which can display 8 grey levels in each sub-field period (M=8) in accordance with the first method when n=3, A=1, and B=1. According to formula (2), the ratio of durations of the display periods SP1 through SP3 of the sub-field periods SF1 through SF3 is

$$1:8-1:(8-1)\times 8 = 1:7:56.$$

At this time, the number of displayable grey levels is 512.

In this case, it is considered that a large shift in the mean position of the bright display periods occurs, for example, on the following occasions:

① at a transition of the display level from level 6 to level 7, or from level 7 to level 8; and

② at a transition of the display level from level 55 to level 56, or from level 56 to level 57.

In these occasions, the largest shift in the mean position of the bright display periods occurs at ②, namely the transition of display level from level 55

to level 56, or from level 56 to level 57.

According to an example shown in Figs. 6(a) through 6(d), in the display state of level 55, the display periods SP1 and SP2 of sub-field periods SF1 and SF2 are in the ON-state (see Fig. 6(a)). In the display state of level 57, the display periods SP1 and SP3 of sub-fields SF1 and SF3 are in the ON-state (see Fig. 6(d)). As the display state of level 56, both of the redundant emission pattern shown in Fig. 6(b) and the conventional emission pattern of Fig. 6(c) exist. In these figures, the numeric values on the vertical axis indicate the pixel division grey level ratio (grey levels due to spatial dither). For example, in the sub-field period SF1 of Fig. 6(a), the pixel is in the state shown in Fig. 3(g).

Thus, the largest shift in the mean position of the bright display periods occurs at a transition from level 55 to level 56 of the conventional emission pattern and a transition from level 56 of the redundant emission pattern to level 57.

Therefore, when displaying level 56, it is judged whether the previous display state is a level not higher than level 55 or a level not lower than level 57. If the previous display state is a level not higher than level 55, the redundant emission pattern

shown in Fig. 6(b) is used as level 56. On the other hand, if the previous display state is a level not lower than level 57, the conventional emission pattern shown in Fig. 6(c) is used. With this structure, it is possible to limit the shift in the mean position of the display periods.

Similarly, although not shown in the drawings, when n=3, A=2 and B=1, the ratio of durations of the display periods SP1 through SP3 of the sub-field periods SF1 through SF3 is

$$1:8:(8^2-1) = 1:8:63,$$

then a similar result is obtained when the display state changes from level 62 to level 63, or from level 63 to level 64.

Fig. 7 shows a time division grey-scale display produced by a combination of the first and second methods. More specifically, here, a single data electrode is divided into two sub-data-electrodes so that the ratio of the electrode widths is 1:2, and the second method in which the brightness of the pixel is changed by controlling the pulse voltage to be applied to the data electrode only in a sub-field period corresponding to the lowest-order bit is used. In this case, in the sub-field periods corresponding to bits other than the lowest-order bit, only a 4-grey-

scale display is produced in each of the sub-field periods corresponding to the bits other than the lowest-order bit, and a 19-grey-scale display is provided only in a sub-field period corresponding to the lowest-order bit.

According to the example shown in Fig. 7, in the sub-field periods corresponding to the bits other than the lowest-order bit, only 4 grey levels are displayable, then M=4. At this time, n=3, A=1, and B=1. In Fig. 7, a single "o" of SD1 (the area ratio = 1) shows 7 grey levels of 0, 1, 2, 3, 4, 5, 6, while a single "o" of SD2 (the area ratio = 2) shows 7 grey levels of 0, 2, 4, 6, 8, 10, 12. Thus, 19 (0 through 18) grey levels are displayed in total.

According to formula (2), the ratio of durations of the display periods of the sub-field periods SF1 through SF3 is

$$1:(4-1):(4-1)\times 4 = 1:3:12.$$

At this time, the number of grey levels that can be displayed is 49 (or 289 if the number of grey levels of the lowest-order bit is taken into account).

In this case, it is considered that a large shift in the mean position of the bright display periods occurs, for example, on the following occasions:

① at a transition of the display level from

level 17 to level 18, or from level 18 to level 19;

② at a transition of the display level from level 71 to level 72, or from level 72 to level 73; and

③ at a transition of the display level from level 141 to level 142, or from level 142 to level 143.

In these occasions, the largest shift in the mean position of the bright display periods occurs at ②, namely the transition of display level from level 71 to level 72, or from level 72 to level 73.

According to the example shown in Fig. 7, in the display state of level 71, the display periods SP1 and SP2 are in the ON-state (see the upper left of Fig. 8). In the display state of level 73, the display periods SP1 and SP3 are in the ON-state (see the lower left of Fig. 8). As the display state of level 72, both of the conventional emission pattern shown in the right center of Fig. 8 and the redundant emission pattern shown in the left center are present.

Thus, the largest shift in the mean position of the bright display periods occurs at a transition from level 71 to level 72 of the conventional emission pattern and a transition from level 72 of the redundant emission pattern to level 73.

Therefore, when displaying level 72, it is judged whether the previous display state is a level not higher than level 71 or a level not lower than level 73. If the previous display state is a level not higher than level 71, the redundant emission pattern shown in the left center of Fig. 8 is used. On the other hand, if the previous display state is a level not lower than level 73, the conventional emission pattern shown in the right center of Fig. 8 is used. With this structure, it is possible to limit the shift in the mean position of the display periods.

As described above, in the display device of this embodiment for producing a multi-grey-scale display by forming one field from a plurality of sub-fields which are different from each other in durations of display periods, the ratio of durations of the display periods of the respective sub-field periods is arranged to satisfy above-mentioned formula (2) or (3).

With this arrangement, for example, when n=3, A=1, and B=1, the number of displayable grey levels is 512, thereby reducing the problems such as spurious noise and false contour associated with the time division grey-scale display. When the number of sub-fields is 3 (n=3), 584 grey levels can be displayed by the time division grey-scale display with a ratio of

durations of the display periods of 1:8:64 according to a conventional technique. However, according to the high-order-bit division technique, the number of grey levels displayable by the time division grey-scale display with a ratio of durations of the display periods of 1:4:4 is only 72. Similarly, with the sub-fields relocation technique, the number of grey levels displayable by the time division grey-scale display with a ratio of durations of the display periods of 4:1:4 is only 72. At this time, with the lowest-order bit addition technique, the number of grey levels displayable by the time division grey-scale display with a ratio of durations of the display periods of 1:1:8 is only 80. Whereas according to this embodiment, the number of grey levels displayable by the time division grey-scale display with a ratio of durations of the display periods of 1:7:56 is 512. It can thus be understood that when the same number of sub-fields is used, the number of displayable grey levels by the structure of the present invention is significantly increased as compared with the high-order-bit division technique, sub-fields relocation technique, and lowest-order bit addition technique.

Moreover, when M=4, n=3, A=1 and B=1, the number of displayable grey levels is given by 16x3+2=49 (or

16x3x6+1=289 if the number of grey levels of the lowest-order bit is taken into account), thereby reducing the problems such as spurious noise and false contour associated with the time division grey-scale display. When the same number of sub-fields is used (n=3), 21x3+1=64 grey levels are displayable by the time division grey-scale display with a ratio of durations of the display periods of 1:4:16 according to the conventional technique. However, with the high-order-bit division technique, only 5x3+1=16 grey levels are displayable by the time division grey-scale display with a ratio of durations of the display periods of 1:2:2. Similarly, with the sub-fields relocation technique, only 16 grey levels are displayable by the time division grey-scale display with a ratio of durations of the display periods of 2:1:2. With the lowest-order bit addition technique, only 6x3+1=19 grey levels are displayable by the time division grey-scale display with a ratio of durations of the display periods of 1:1:4. In contrast, according to this embodiment, it is possible to display 49 grey levels by the time division grey-scale display with a ratio of durations of the display periods of 1:3:12. Hence, it can be understood that when the same number of sub-fields is used, the number

of displayable grey levels by the structure of the present invention is significantly increased as compared with the high-order-bit division technique, sub-fields relocation technique, and lowest-order bit addition technique.

Besides, when the display periods corresponding to n sub-field periods are denoted by SP1, SP2, ..., SPi, ..., SPn (i being an integer which is not smaller than A+1 but not greater than n), the display device of this embodiment has a first display state (for example, level 55 or 71) in which the display periods SP2 through SPi are bright, and the display periods SP1, SP(i+1) through SPn are dark; a second display state (for example, level 56 or 72 of the redundant emission pattern) in which the display periods SP1 through SPi are bright and the display periods SP(i+1) through SPn are dark, the second display state having a brightness level next to the brightness level of the first display state; a third display state (for example, level 56 or 72 of the conventional emission pattern) in which the display period SP(i+1) is bright and the display periods SP1 through SPi, SP(i+2) through SPn are dark, the third display state having the same brightness level as the second display state; and a fourth display state (for example, level 57 or

73) in which the display periods SP1 and SP(i+1) are bright and the display periods SP2 through SPi, SP(i+2) through SPn are dark, the fourth display state having a brightness level next to the brightness level of the third display state.

Furthermore, when selecting the brightness level of the second or third display state, if the display state in the previous field of each pixel is not higher than the brightness level of the first display state, the second display state is selected as the next display state. On the other hand, if it is not lower than the brightness level of the fourth display state, the third display state is selected as the next display state.

Therefore, a dark image or a bright line is not displayed over one field, thereby preventing degradation of the image quality.

In this embodiment, a single data electrode is divided into three or two sub-data-electrodes. However, the data electrode is not necessarily divided into such a number of sub-data-electrodes. In other words, the number into which a data electrode is divided can be freely selected according to the need.

Above-mentioned Embodiments 1 and 2 are explained with reference to one pixel. Considering a plurality

of pixels as a whole, the shift in the mean position of the display periods can further be limited by the following structure.

Specifically, as illustrated in Fig. 9, when displaying a particular grey level (for example, above-mentioned level 112, 56 or 72) having two patterns, namely the redundant emission pattern and conventional emission pattern, the redundant emission pattern (indicated by ● in Fig. 9) and conventional emission pattern (shown by o in Fig. 9) are selected alternately so that each pattern appears every other line in either of the vertical and horizontal directions. With this structure, when a plurality of pixels are seen as a whole, the shift in the mean position of the display periods can be limited.

Moreover, when displaying a particular grey level (for example, above-mentioned level 112, 56 or 72) having both the redundant emission pattern and conventional emission pattern, the particular grey level and the brightness levels of the surrounding pixels are compared with each other. When many of the surrounding pixels have brightness levels lower than the particular grey level, the redundant emission pattern similar to an emission pattern (the particular grey level - 1) is preferably selected as the display

state of a target pixel. On the other hand, when many of the surrounding pixels have brightness levels higher than the particular grey level, the conventional emission pattern similar to an emission patten (the particular grey level + 1) is preferably selected as the display state of the target pixel. With this structure, when a plurality of pixels are seen as a whole, the shift in the mean position of the display periods can be limited.

Embodiments 1 and 2 describe the FLCDs. However, the same effects can be produced with a PDP if the ratio of durations of the display periods is set in the same manner.

As described above, a first display device of the present invention is a display device for producing a multi-grey-scale display by forming a single field from a plurality of sub-fields which are different from each other in durations of display periods thereof, and arranging the ratio of the durations of the display periods corresponding to the respective sub-fields so that

$$1 : \ldots : 2^m : \ldots : (2^A-B)\times 2^k : \ldots$$

where m represents a variable between 1 and A-1, k represents a variable between 0 and n-A-1, n represents the number of the sub-fields, A represents

an integer of not less than 2, and B represents an integer of not less than 1.

A second display device of the present invention is a display device for producing a multi-grey-scale display by forming a single field from a plurality of sub-fields which are different from each other in durations of display periods thereof and arranging the ratio of the durations of the display periods corresponding to the respective sub-fields so that

$$1 : (M^A-B)\times M^k : \ldots,$$

or

$$1 : \ldots : M^m : \ldots : (M^A-B)\times M^k : \ldots$$

where M (M being an integer of not less than 3) represents the number of grey levels displayable in the sub-field periods corresponding to bits other than the lowest-order bit, m represents a variable between 1 and A-1, k represents a variable between 0 and n-A-1, n represents the number of the sub-fields, A represents an integer of not less than 1, and B represents an integer of not less than 1.

When the structures of the first and second display device are adopted into a device in which each pixel can display two or more grey levels and when the same number of the sub-fields are used in such a display device and conventional devices, if ON/OFF of

the sub-field periods is appropriately controlled according to a change in the brightness of the image in a time-axis direction, the display device adopting the structures of the first and second display devices can exhibit a significantly increased number of grey levels as compared with the conventional structures, without causing problems such as spurious noise and false contour associated with the time division grey-scale display.

Another preferred structure (called the "structure A") is based on the structure of the second display device, and includes a plurality of scanning electrodes arranged parallel to each other;

a plurality of data electrodes arranged parallel to each other and orthogonally to the scanning electrodes;

a liquid crystal layer made of a ferroelectric liquid crystal, placed between the scanning electrodes and the data electrodes; and

pixels formed in matrix by the scanning electrodes and the data electrodes which are arranged to cross each other, each pixel including a plurality of sub-pixels.

With the structure A, since a single pixel is divided into sub-pixels, it is possible to display

three or more grey levels by each pixel. Therefore, the value of M can be freely set, and a suitable number of grey levels is obtained according to the need.

Yet another preferred structure (called the "structure B") is based on the structure of the second display device, and includes a plurality of scanning electrodes arranged parallel to each other;

a plurality of data electrodes arranged parallel to each other and orthogonally to the scanning electrodes;

a liquid crystal layer made of a ferroelectric liquid crystal, placed between the scanning electrodes and the data electrodes; and

pixels formed in matrix by the scanning electrodes and data electrodes which are arranged to cross each other, wherein the brightness of each pixel is changed by control of a pulse voltage to be applied to the data electrodes.

With the structure B, since the ratio of a bright domain area to a dark domain area within a single pixel can vary, a single pixel can display three or more grey levels. Therefore, the value of M can be freely set, and a suitable number of grey levels is obtained according to the need.

Still another preferred structure (called the "structure C") is based on the structure of the second display device, and includes a plurality of scanning electrodes arranged parallel to each other;

a plurality of data electrodes arranged parallel to each other and orthogonally to the scanning electrodes;

a liquid crystal layer made of a ferroelectric liquid crystal, placed between the scanning electrodes and the data electrodes; and

pixels formed in matrix by the scanning electrodes and data electrodes which are arranged to cross each other, wherein each pixel includes a plurality of sub-pixels, and the brightness of each pixel is changed by control of a pulse voltage to be applied to the data electrodes.

Since the structure C is obtained by a combination of the above-mentioned structures A and B, it can produce effects similar to both the effects of structures A and B. Additionally, since the number of grey levels to be displayed can be selected from a wider range, it is possible to set a suitable number of grey levels according to a desired application.

A further preferred structure (called the "structure D") is based on any of the first and second

display devices and the structures A, B, C, and when display periods corresponding to n sub-field periods are represented by SP1, SP2, ..., SPi, ..., SPn (i being an integer which is not smaller than A+1 but not greater than n), the structure D includes:

a first display state in which the display period SP1 is a grey level, the display periods SP2 through SPi are bright, and the display periods SP(i+1) through SPn are dark;

a second display state in which the display periods SP1 through SPi are bright and the display periods SP(i+1) through SPn are dark, the second display state having a brightness level next to a brightness level of the first display state;

a third display state in which the display period SP(i+1) is bright and the display periods SP1 through SPi, SP(i+2) through SPn are dark, the third display state having the same brightness level as the second display state; and

a fourth display state in which the display period SP1 is a grey level, the display period SP(i+1) is bright, and the display periods SP2 through SPi, SP(i+2) through SPn are dark, the fourth display state having a brightness level next to the brightness level of the third display state.

According to the structure D, there are two display states of the same brightness level. Therefore, if a display state is appropriately selected from the two display states according to a change in the brightness of an image, it is possible to minimize the shift in the mean position of the display periods.

In the structure of D, when selecting the brightness level of the second or third display state, if a display state in the previous field of each pixel is not higher than the brightness level of the first display state, the second display state is preferably selected as the next display state. On the other hand, if the display state in the previous field is not lower than the brightness level of the fourth display state, the third display state is preferably selected as the next display state.

With this structure, since a dark image or a bright line is not displayed over one field, it is possible to prevent degradation of the image quality.

Moreover, in the structure D, it is preferred to arrange the display states of adjacent pixels to differ from each other by using the second and third display states.

With this arrangement, since a pixel of the

second display state and a pixel of the third display state are located adjacent to each other, when a plurality of pixels are seen as a whole, the shift in the mean position of the display periods can be limited.

Furthermore, in the structure D, when selecting the second or third display state as the display state of a particular pixel, if the display states of pixels surrounding the particular pixel are not higher than the brightness level of the first display state, the display state of the particular pixel is preferably made the second display state. On the other hand, if the display states of the surrounding pixels are not lower than the brightness level of the fourth display state, the display state of the particular pixel is preferably made the third display state.

With this structure, since the display state of the particular pixel is selected after making a comparison with the surrounding pixels, when a plurality of pixels are seen as a whole, the shift in the mean position of the display periods can be limited.

The invention being thus described, it will be obvious that the same may be varied in many ways. Such variations are not to be regarded as a departure from

the spirit and scope of the invention, and all such modifications as would be obvious to one skilled in the art are intended to be included within the scope of the following claims.

CLAIMS:

1. A display device for providing a multi-grey-scale display by forming a single field from a plurality of sub-fields which are different from each other in durations of display periods thereof,

wherein a ratio of the durations of the display periods corresponding to the respective sub-fields is arranged so that

$1: \ldots : 2^m : \ldots : (2^A-B)\times 2^k : \ldots$

where m represents a variable between 1 and A-1, k represents a variable between 0 and n-A-1, n represents the number of the sub-fields, A represents an integer of not less than 2, and B represents an integer of not less than 1.

2. The display device as set forth in claim 1,

wherein when display periods corresponding to n sub-fields periods are represented by SP1, SP2, ..., SPi, ..., SPn (i being an integer which is not smaller than A+1 but not greater than n), said display device comprises:

a first display state in which the display periods SP2 through SPi are bright and the display periods SP1, SP(i+1) through SPn are dark;

a second display state in which the display

periods SP1 through SPi are bright and the display periods SP(i+1) through SPn are dark, the second display state having a brightness level next to a brightness level of the first display state;

a third display state in which the display period SP(i+1) is bright and the display periods SP1 through SPi, SP(i+2) through SPn are dark, the third display state having the same brightness level as the second display state; and

a fourth display state in which the display periods SP1 and SP(i+1) are bright and the display periods SP2 through SPi, SP(i+2) through SPn are dark, the fourth display state having a brightness level next to the brightness level of the third display state.

3. The display device as set forth in claim 2,

wherein when selecting the brightness level of the second or third display state, if a display state in a previous field of each pixel is not higher than the brightness level of the first display state, the second display state is selected as a next display state, and if the display state in the previous field of each pixel is not lower than the brightness level of the fourth display state, the third display state

is selected as the next display state.

4. The display device as set forth in claim 2,

wherein display states of adjacent pixels are arranged to differ from each other using the second display state and third display state.

5. The display device as set forth in claim 2,

wherein when setting a display state of a particular pixel as the second or third display state, if display states of pixels surrounding said particular pixel are not higher than the brightness level of the first display state, the display state of said particular pixel is made the second display state, and if the display states of the pixels surrounding said particular pixel are not lower than the brightness level of the fourth display state, the display state of said particular pixel is made the third display state.

6. A display device for providing a multi-grey-scale display by forming a single field from a plurality of sub-fields which are different from each other in durations of display periods thereof,

wherein a ratio of the durations of the display

periods corresponding to the respective sub-fields is arranged so that

$$1 : (M^A - B) \times M^k : \ldots,$$

or

$$1 : \ldots : M^m : \ldots : (M^A - B) \times M^k : \ldots$$

where M (M being an integer of not less than 3) represents the number of grey levels displayable in a sub-field period corresponding to each bit except a lowest-order bit, m represents a variable between 1 and A-1, k represents a variable between 0 and n-A-1, n represents the number of the sub-fields, A represents an integer of not less than 1, and B represents an integer of not less than 1.

7. The display device as set forth in claim 6, comprising:

a plurality of scanning electrodes arranged parallel to each other;

a plurality of data electrodes arranged parallel to each other and orthogonally to said scanning electrodes;

a liquid crystal layer including a ferroelectric liquid crystal, placed between said scanning electrodes and said data electrodes; and

pixels formed in matrix by said scanning

electrodes and said data electrodes which are arranged to cross each other, each pixel including a plurality of sub-pixels.

8. The display device as set forth in claim 6, comprising:

a plurality of scanning electrodes arranged parallel to each other;

a plurality of data electrodes arranged parallel to each other and orthogonally to said scanning electrodes; and

a liquid crystal layer including a ferroelectric liquid crystal, placed between said scanning electrodes and said data electrodes,

pixels formed in matrix by said scanning electrodes and said data electrodes which are arranged to cross each other, a brightness of each pixel being changed by control of a pulse voltage to be applied to said data electrodes.

9. The display device as set forth in claim 6, comprising:

a plurality of scanning electrodes arranged parallel to each other;

a plurality of data electrodes arranged parallel

to each other and orthogonally to said scanning electrodes;

a liquid crystal layer including a ferroelectric liquid crystal, placed between said scanning electrodes and said data electrodes; and

pixels formed in matrix by said scanning electrodes and said data electrodes which are arranged to cross each other, each pixel including a plurality of sub-pixels, a brightness of each pixel being changed by control of a pulse voltage to be applied to said data electrodes.

10. The display device as set forth in claim 6, wherein when display periods corresponding to n sub-field periods are represented by SP1, SP2, ..., SPi, ..., SPn (i being an integer which is not smaller than A+1 but not greater than n), respectively, said display device comprises:

a first display state in which the display periods SP2 through SPi are bright and the display periods SP(i+1) through SPn are dark;

a second display state in which the display periods SP1 through SPi are bright and the display periods SP(i+1) through SPn are dark, the second display state having a brightness level next to a

brightness level of the first display state;

a third display state in which the display period SP(i+1) is bright and the display periods SP1 through SPi, SP(i+2) through SPn are dark, the third display state having the same brightness level as the second display state; and

a fourth display state in which the display period SP(i+1) is bright and the display periods SP2 through SPi, SP(i+2) through SPn are dark, the fourth display state having a brightness level next to the brightness level of the third display state.

11. The display device as set forth in claim 10,

wherein when selecting the brightness level of the second or third display state, if a display state in a previous field of each pixel is not higher than the brightness level of the first display state, the second display state is selected as a next display state, and if the display state in the previous field of each pixel is not lower than the brightness level of the fourth display state, the third display state is selected as the next display state.

12. The display device as set forth in claim 10,

wherein display states of adjacent pixels are

arranged to differ from each other using the second display state and third display state.

13. The display device as set forth in claim 10, wherein when setting a display state of a particular pixel as the second or third display state, if display states of pixels surrounding said particular pixel are not higher than the brightness level of the first display state, the display state of said particular pixel is made the second display state, and if the display states of the pixels surrounding said particular pixel are not lower than the brightness level of the fourth display state, the display state of said particular pixel is made the third display state.

The Patent Office

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Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.P): G5C (CHB)

Int Cl (Ed.6): G09G 3/28 3/36

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Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
P,X	GB 2318248 A	MITSUBISHI see page 19 lines 7-15, page 24 line 1 to page 29 line 4, and page 31 lines 1-9	1, 2, 4
A	GB 2307325 A	SHARP	6-13
A	EP 0774745 A2	MATSUSHITA	

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